REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants have amended Claims 1 and 49 to positively recite that the buried oxide region formed has a thickness from about 1000 to about 2000 Å. Support for this amendment to the claims is found on Page 7, line 19 of the originally filed application.

Applicants have also amended Claims 1 and 49 by deleting the optical detecting step from the present claims since the same is not needed for patentability.

Applicants respectfully submit that the above amendments to the claims do not introduce new matter to the specification of the instant application. Applicants thus respectfully request entry of the above amendments to the claims.

In the present Office Action, Claims 1, 3-22, 25-36, 40 and 48, 49 and 51-52 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of U.S. Patent No. 6,090,689 to Sadana, et al. ("Sadana '689"), U.S. Patent No. 5,534,446 to Tachimori, et al. ("Tachimori, et al.") and U.S Patent No. 5,930,643 to Sadana, et al. ("Sadana '643") and/or admitted prior art.

Applicants respectfully submit that the combined disclosures of Sadana '689, Tachimori, et al., Sadana '643 and/or the admitted prior art do not render the claimed methods obvious. Specifically, Sadana '689, Tachimori, et al., Sadana '643 and/or the admitted prior art do not teach or suggest applicants' claimed methods which include processing steps that are capable of forming a semiconductor-on-insulator having a superficial Si-containing layer having a thickness from about 100 to about 2000 Å that is separated from a bottom Si-containing layer by a buried oxide having a thickness from

about 1000 to about 2000 Å, wherein the tile or divot defects present at a top surface of said superficial Si-containing layer have a first density that does not obstruct detection of other defects that have a second density that is lower than said first density. The formation of such an SOI substrate having all of the above mentioned features is not taught or suggested in the art without a piecemeal reconstruction.

Applicants observe that Sadana '689 provides a SOI substrate including a continuous oxide layer 22 having a thickness of 0.07 μm (i.e., 700 Å) that includes no visible Si inclusion from the overlaying Si-containing layer. See Col. 5, lines 20-21. Moreover at Col. 5, lines 24-27, Sadana '689 discloses that the interface between the oxide layer 22 and the Si overlayer is somewhat undulated with defects including twins and pyramidal stacking faults that extend into the Si overlayer. Sadana '689 further states at Col. 5, lines 27-30 that the process disclosed therein provides a SOI substrate that has a low density of threading dislocations extending about 0.05 μm into the Si overlayer, i.e., from the buried oxide into the Si overlayer. Applicants further observe that at Col. 6, lines 12-15 Sadana '689 discloses that a deposited silicon oxide layer formed atop the substrate 12 prior to ion implantation can make the final Si wafer smoother.

Sadana '689 does not report the thickness of the superficial Si-containing layer therefore the applied reference does not disclose the claimed range of about 100 to about 2000 Å. Applicants further observe that the term "tile defects" or "divot defects" does not appear anywhere in the disclosure of Sadana '689 and that the defects disclosed in the prior art, which are mainly said to be at or near the interface between the buried oxide and the Si overlayer, are different from tile or divot defects that are recited to be present at the upper, i.e., top, surface of the Si-containing overlayer. Indeed, as is known to one

skilled in the art, a threading defect, stacking fault or twin defect present at the interface between the Si-containing overlayer and the buried oxide layer is different from a tile or divot defect that is present at the upper surface of the Si-containing overlayer. Applicants submit that the top surface referred to in the claims is distant from the interface referred to in Sadana '689.

Applicants also submit that a smooth surface, as referred to in the Sadana '689 disclosure, does not necessarily equate to a *superficial Si-containing having an upper surface including a number of tile defects or divot defects having a first density that does not obstruct detection of other defects that have a second density that is lower than the first density*. That is, it is possible to have a smooth surface with a high number of tile defects that can inhibit the detection of the other defects that have a lower density that the tile or divot defects.

Applicants further submit that the defects referred to in Sadana '689 are defects that have a lower density than the tile or divot defects presently claimed. Moreover, the defects disclosed in Sadana '689 are atomic scale defects that cannot be detected without highlighting. Applicants submit that the other defects mentioned in the claimed invention are process induced defects not atomic scale defects as disclosed in Sadana '689. Applicants respectfully submit that Sadana '689, as exemplified by the above mentioned text, does not disclose the claimed SOI substrate that includes a superficial Si-containing layer having a thickness from about 100 to about 2000 Å and a buried oxide having a thickness from about 1000 to about 2000 Å, said superficial Si-containing layer having an upper surface including a number of tile defects or divot defects having a first density that does not obstruct detection of other defects that have a second density that is lower than the first density.

Tachimori, et al. also do not teach or suggest a method of forming a SOI substrate material which is capable of reducing the tile or divot defects in a superfacial Si-containing layer having a thickness from about 100 to about 2000 Å, which is located atop a buried oxide having a thickness from about 1000 to about 2000 Å, as presently claimed. The objective in Tachimori, et al. is to provide a process for forming an SOI substrate material in which the conditions are capable of increasing the thickness of the buried oxide, while extinguishing the defects lacking in oxygen atoms in the buried oxide. The Tachimori, et al. process utilizes a single implant and the anneal is performed utilizing a partial pressure of oxygen of about $5x10^3$ Pa or more. Applicants note that in their claimed invention a two step implant process is recited and because no recitation is given in either the specification or claims of the partial pressure of oxygen, a normal pressure is used. Applicants submit that the combined disclosures of Sadana '689 and Tachimori, et al. would result in a method of forming an SOI substrate utilizing at least the low temperature anneal disclosed in Sadana, et al. prior to a second higher temperature anneal, wherein at least one of the anneals includes the partial pressure of oxygen recited in Tachimori, et al. Applicants observe that the prior art disclosed in Tachimori, et al. uses a single implant and a normal O_2 pressure anneal.

Applicants further submit that Tachimori, et al. does not teach or suggest annealing a substrate containing the implanted oxygen ions in an ambient gas that comprises from about 0 to about 90% oxygen and from about 10 to about 100% of N_2 at a temperature of about 1250°C or greater to form a buried oxide region which electrically isolates a superficial Si-containing layer having a thickness from about 100 to about 2000 Å from a bottom Si-containing layer, wherein said annealing is carried out until tile or divot defects present at a top surface of said superficial Si-containing layer have a first

density that does not obstruct detection of other defects that have a second density that is lower than said first density. The process of the prior art merely addresses defects present in the buried oxide and is not concerned with defects that may be present in the SOI layer of the substrate.

Sadana '643 provides a method of forming a defect induced buried oxide in which the defect induced buried oxide has improved electrical qualities. There is no disclosure in Sadana '643 which teaches or suggest a method of forming a SOI substrate material which is capable of reducing the tile or divot defects in a superfacial Si-containing layer having a thickness from about 100 to about 2000 Å and a buried oxide having a thickness from about 1000 to about 2000 Å, as presently claimed. Applicants observe that defects mentioned in '643 are similar to those discussed above in Sadana '689.

Finally, it is not inherent that annealing a substrate containing the implanted oxygen ions in an ambient gas that comprises from about 0 to about 90% oxygen and from about 10 to about 100% of N_2 at a temperature of about 1250°C or greater forms a buried oxide region which electrically isolates a superficial Si-containing layer having a thickness from about 100 to about 2000 Å from a bottom Si-containing layer, wherein said annealing is carried out until tile or divot defects present at a top surface of said superficial Si-containing layer have a first density that does not obstruct detection of other defects that have a second density that is lower than said first density, using the process steps disclosed by the applied references, including Sadana '643, Sadana '689, and Tachimori, et al. The Federal Circuit has held that inherency cannot be based on mere speculation. *See e.g., Continental Can Co. USA, Inc. v. Monsanto Co.*, 848 F.2d 1264, 1269, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991) (inherency "may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a

given set of circumstances is not sufficient.") When anticipation is based on inherency of limitations not expressly disclosed in the assertedly anticipating reference, it must be shown that the undisclosed information was known to be present in the subject matter of the reference. See *Elan Pharmaceuticals, Inc., v. Mayo Foundation for Medical Education and Research*, 304 F.3d 1221, 1228, 64 USPQ2d 1292 (Fed. Cir. 2002) (*citing Continental Can*, 948 F.2d at 1269). The alleged limitation must be necessarily present so that one of ordinary skill would recognize its presence. *Crown Operations International, LTD v. Solutia Inc.*, 289 F.3d 1367, 1377, 62 USPQ2d 1917 (Fed. Cir. 2002). 'The mere fact that a certain thing may result from a given set of circumstances is not sufficient [to establish inherency.]' ... 'That which may be inherent is not necessarily known. Obviousness cannot be predicated on what is unknown.' ' *In re Rijckaet* 9 F.3d 1534, 28 USPQ2d at 1957.

The court in *Elan Pharmaceuticals v. Mayo Foundation for Medical Education and Research* held that when a rejection is based on inherency of limitations not expressly disclosed in the assertedly anticipating reference, it must be shown that the undisclosed information was known to be present in the subject matter of the reference. See *Elan Pharmaceuticals, Inc., v. Mayo Foundation for Medical Education and Research*, 304 F.3d 1221, 1228, 64 USPQ2d 1292 (Fed. Cir. 2002) (*citing Continental Can*, 948 F.2d at 1269). In *Elan Pharmaceuticals* the claim limitation at issue before the court was, "wherein said polypeptide is processed to ATF-betaAPP in a sufficient amount to be detectable in a brain homogenate of said transgenic rodent". It was undisputed that the applied reference made no reference to the formation of "ATF-betaAPP". The court found that the Examiner's applied references were no more than broad teachings and were not directed to the applicants' claimed limitation. *Id. at* 1228. The referenced prior

art was described as merely "an invitation to experiment with no assurances of success" *Id.* Finally, the court stated that a general recitation of known procedures does not defeat the novelty of the invention as produced by the applicant.

Similar to the prior art examined in *Elan Pharmaceuticals*, the referenced prior art cited in the present Office Action does not teach or suggest all of the claimed limitations of the invention. "Facts asserted to be inherent in the prior art must be shown by evidence from the prior art". In re Dembiczak, 175 F.3d 949, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999) (criticizing the hindsight syndrome wherein that which only the inventor taught is used against its teacher). Neither, Tachimori, et al. nor the Sadana, et al. references teach or suggest tile or divot defects, as recited in amended Claims 1 and 49, let alone that that claimed method in which the annealing step is carried out until tile or divot defects present at a top surface of said superficial Si-containing layer have a first density that does not obstruct detection of other defects that have a second density that is lower than said first density.

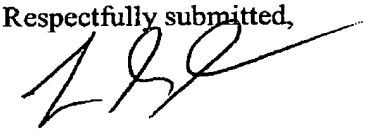
Additionally, the combined references of Tachimori, et al. and the Sadana, et al. references, similar to the prior art discussed in *Elan Pharmaceuticals*, at most disclose a general recitation of procedures that were not carried out in a manner in which one of ordinary skill in the art would recognize the unexpected advantages in tile or divot defect reduction achieved using applicants' method, recited in amended Claims 1 and 49. Therefore, in light of the holding of *Elan Pharmaceuticals,* applicants' method recited in amended Claims 1 and 49 is not obvious.

In light of the standard established by the Federal Circuit, applicants respectfully request that the § 103 rejection be withdrawn.

Based on the above amendments and remarks, the rejection to the claims under 35 U.S.C. § 103 have been obviated; therefore reconsideration and withdrawal of the instant rejection are respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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